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AD1855

Stereo, 96KHz, Multibit ΣΔ DAC

PRELIMINARY INFORMATION

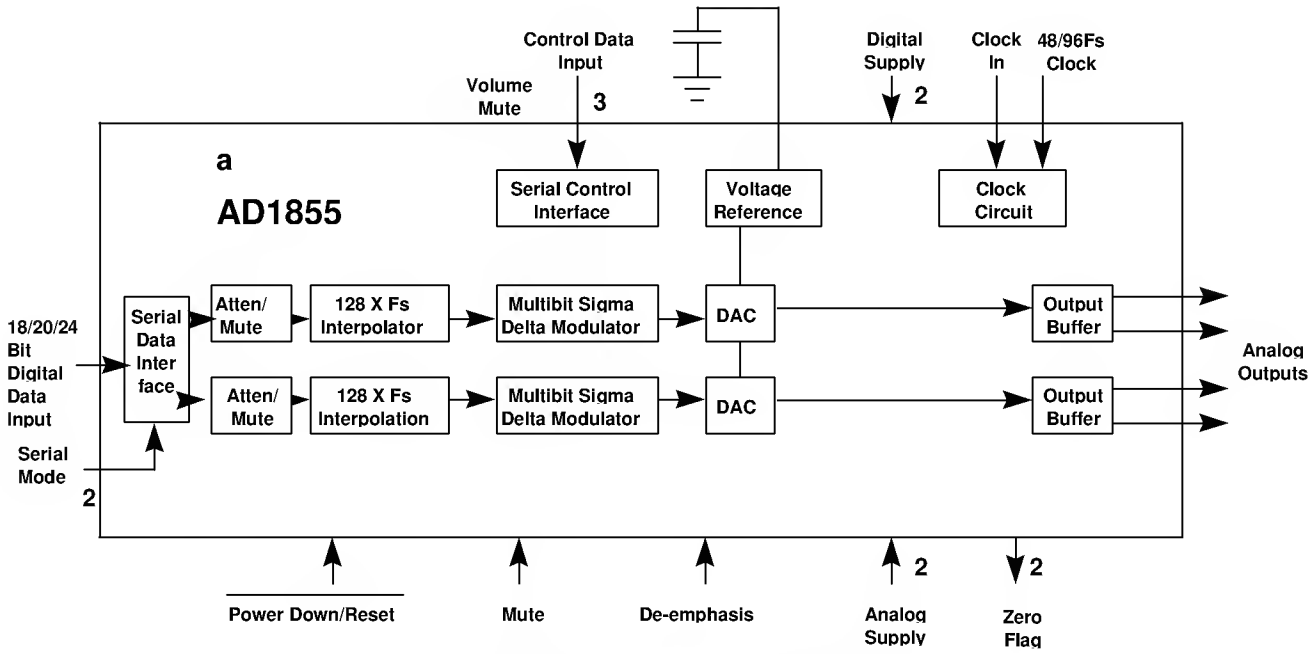
Rev 0.7 9/30/97

FEATURES

5V Stereo Audio DAC System. Accepts 16/18 /20/24-Bit Data
Supports 24-Bits and 96Khz Sample Rate
Multibit Sigma Delta Modulator with "Perfect Differential Linearity Restoration" for Reduced Idle Tones and Noise Floor
Data Directed Scrambling DAC - Least Sensitive to Jitter
Differential Output for Optimum Performance
113 dB Dynamic Range at 48KHz Sample Rate
110 dB Dynamic Range at 96KHz Sample Rate
-100dB THD+N Performance Target
On-chip Volume Control With 1024 Steps
Hardware and Software Controllable Clickless Mute
Zero Input Flag Outputs For Left and Right Channels
Digital De-emphasis Processing
Supports 256 X Fs or 384 X F_S Master Mode Clock
Switchable Clock Doubler
Power Down Mode Plus Soft Power Down Mode
Flexible Serial Data Port with Right-Justified, Left-Justified, I^2S-Compatible and DSP Serial Port Modes
28 Lead SSOP Plastic Package

APPLICATIONS

DVD, CD, Set-top Boxes, Home Theater Systems, Automotive Audio Systems, Computer Multimedia Products, Sampling Musical Keyboards, Digital Mixing Consoles, Digital Audio Effects Processors



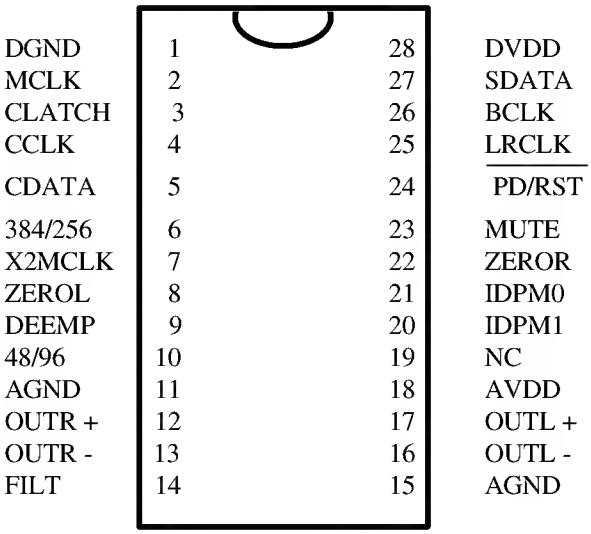
AD1855 Block Diagram

a AD1855

PRODUCT OVERVIEW

The AD1855 is a complete 18/20/24-bit single-chip stereo digital audio playback system. It is comprised of a multibit sigma-delta modulator with dither, continuous time analog filters, and analog output drive circuitry. Other features include an on-chip stereo attenuator and mute, programmed through an SPI-compatible serial control port. The AD1855 is fully compatible with all known DVD formats including 96kHz sample frequency and 24-bits. It also is backwards compatible by supporting 50/15µs digital de-emphasis intended for "redbook" 44.1kHz sample frequency playback from Compact Discs.

The AD1855 has a very simple but very flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSP chips, AES/EBU receivers and sample rate converters. The AD1855 can be configured in Left-justified, I^2S, Right-Justified, or DSP serial port compatible modes. The AD1855 accepts serial audio data in MSB first, twos-compliment format. A power-down mode is offered to minimize power consumption when the device is inactive. The AD1855 operates from a single +5 V power supply. It is fabricated on a single monolithic integrated circuit and is housed in a 28-pin SSOP packages for operation over the temperature range 0^0C to +70^0C.



NC = No Connect

AD1855 PINOUT

NOTE: This preliminary pinout is subject to change

PIN DESCRIPTION **AD1855**

Pin	Input/Output	Pin Name	Description
14	O	FILT	Voltage Reference Filter Capacitor connection. Bypass and decouple the voltage reference with parallel 10 µF and 0.1 µF capacitors to the AGND.
9	I	DEEMP	De-emphasis. Digital de-emphasis is enabled when this input signal is HI. This is used to impose a 50/15 ms response characteristic on the output audio spectrum at an assumed 44.1 kHz sample rate.
8	O	ZEROL	Left Channel Zero Flag output. This pin goes HI when Left Channel has no signal input for more than 1024 LR Clock Cycles.
17	O	OUTL +	Left Channel Positive line level analog output.
16	O	OUTL -	Left Channel Negative line level analog output.
11,15	I	AGND	Analog Ground.
23	I	MUTE	Mute. Assert HI to mute both stereo analog outputs. Deassert LO for normal operation.
21	I	IDPM0	Input serial data port mode control zero. With IDPM1, defines 1 of 4 serial modes.
20	I	IDPM1	Input serial data port mode control one. With IDPM0, defines 1 of 4 serial modes.
24	I	PD/RST	Power down/reset. The AD1855 is placed in a low power consumption mode when this pin is held LO. The AD1855 is reset on the rising edge of this signal. The serial control port registers are reset to the default values. Connect HI for normal operation.
27	I	SDATA	Serial input, MSB first, containing two channels of 16/18/20/24 bits of twos compliment data per channel.
25	I	LRCLK	Left/Right clock input for input data. Must run continuously.
26	I	BCLK	Bit clock input for input data. Need not run continuously; may be gated or used in a burst fashion.
10	I	48/96	Selects 48 kHz (LO) or 96kHz Sample Frequency Control.
2	I	MCLK	Master Clock Input. Connect to an external clock source at either 256, 384 or 512 Fs
28	I	DVDD	Digital Power Supply Connect to digital +5 V supply.
1	I	DGND	Digital Ground
4	I	CCLK	Control clock input for control data. Control input data must be valid on the rising edge of CCLK. CCLK may be continuos or gated.
5	I	CDATA	Serial control input, MSB first, containing 16 bits of unsigned data per channel. Used for specifying channel specific attenuation and mute.
3	I	CLATCH	Latch input for control data. This input is rising edge sensitive.
19	-	NC	No Connect. Reserved. Do not connect.
18	I	AVDD	Analog Power Supply. Connect to analog +5 V supply.
12	O	OUTR +	Right Channel Positive line level analog output.
13	O	OUTR -	Right Channel Negative line level analog output.
22	O	ZEROR	Right Channel Zero Flag output. This pin goes HI when Right Channel has no signal input for more than 1024 LR Clock Cycles.
6	I	384/256	Selects the master clock mode as either 384 times the intended sample frequency (HI) or 256 times the intended sample frequency (LO). The state of this input should be hardwired to logic HI or logic LO or may be changed while the AD1855 is in power-down/reset. It must not be changed while the AD1855 is operational.
7	I	X2MCLK	Selects internal clock doubler (LO) or internal clock = MCLK (HI).

SERIAL DATA INPUT MODE

MODE1 (PIN 9)	MODE0 (PIN10)	Serial Data Input Format
0	0	Right-Justified (16 bits only)
0	1	I2S Compatible
1	0	Left-Justified
1	1	DSP

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages (AV_{DD}, DV_{DD})	+5.0V
Ambient Temperature	$25^{O}C$
Input Clock	11.2896MHz (256XFs Mode)
Input Signal	1.0013kHz -0.5 dB Full Scale
Input Sample Rate	44.1kHz
Measurement Bandwidth	20 Hz to 20KHz
Word Width	20 bits
Load Capacitance	100 pF
Load Impedance	47 k ohms
Input Voltage HI	2.4 V
Input Voltage LO	0.8 V

Performance of right and left channels are identical (exclusive of the Interchannel Gain Mismatch and Interchannel Phase Deviation specifications).
Values in **bold** typeface are tested, all others are guaranteed, not tested.

ANALOG PERFORMANCE

	Min	**Typ**	**Max**	**Units**
Resolution		20		Bits
Dynamic Range (20 Hz to 20 kHz, -60 dB Input)				
No Filter		110		dB
With A-Weighted Filter		113		dB
Total Harmonic Distortion + Noise		-97		dB
		.001		%
Analog Outputs				
Differential Output range (+/- Full Scale)		2.8		V P-to-P
Output Impedance at Each Output Pin		<200		Ohms
Output Capacitance at Each Output Pin			20	pF
Out-of-Band Energy (0.5XFs to 100 kHz)			-72.5	dB
CMOUT		2.25		V
DC Accuracy				
Gain Error		+/- 3.0		%
Interchannel Gain Mismatch		0.01		dB
Gain Drift		150		$ppm/^{O}C$
Intercahnnel Crosstalk (EIAJ method)		-120		dB
Interchannel Phase Deviation		+/- 0.1		Degrees
Mute Attenuation		-100		dB
De-emphasis Gain Error			+/- 0.1	dB

DIGITAL I/O

	Min	**Typ**	**Max**	**Units**
Input Voltage HI (V_{IH})	2.4			V
Input Voltage LO (V_{IL})			0.8	V
Input Leakage (I_{IH}@V_{IH}=2.4 V)			10	uA
Input Leakage (I_{IL}@V_{IL}=0.8 V)			10	uA

Input Capacitance			20	pF

POWER

	Min	Typ	Max	Units
Supplies				
Voltage, Analog and Digital	4.75	5	5.25	V
Analog Current			50	mA
Analog Current - Power-Down			60	uA
Digital Current			25	mA
Digital Current - Power-Down				
Dissipation				
Operation - Both Supplies		375		mW
Operation - Analog Supply		250		mW
Operation - Digital Supply		125		mW
Power-Down - Both Supplies			60mW	mW
Power Supply Rejection Ratio				
1kHz 300 mV p-p Signal at Analog Supply Pins		-60		dB
20kHz 300 mV p-p Signal at Analog Supply Pins		-50		dB

TEMPERATURE RANGE

	Min	Typ	Max	Units
Specifications Guaranteed		25		^{O}C
Functionality Guaranteed	0		70	^{O}C
Storage	-55		125	^{O}C

ABSOLUTE MAXIMUM RATINGS*

	Min	Typ	Max	Units
DV_{DD} to DGND	-0.3		6	V
AV_{DD} to AGND	-0.3		6	V
Digital Inputs	DGND - 0.3		DV_{DD} + 0.3	V
Analog Outputs	AGND - 0.3		AV_{DD} + 0.3	V
AGND to DGND	-0.3		0.3	V
Reference Voltage			$(AV_{DD} + 0.3)/2$	
Soldering			+300	^{O}C
			10	sec

* Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE CHARACTERISTICS

	Min	Typ	Max	Units
O_{JA} (Thermal Resistance [Junction-to-Ambient])		190.87		$^{O}C/W$
O_{JC} (Thermal Resistance [Junction-to-Case])		15.52		$^{O}C/W$

ORDERING GUIDE

Model	Temperature	Package Description	Package Option*
AD1855JRS	0 ^{O}C to +70 ^{O}C	28-Lead SSOP	RS-28
AD1855JRSRL	0 ^{O}C to +70 ^{O}C	28-Lead SSOP	RS-28 on 13” Reels

*RS = Shrink Small Outline